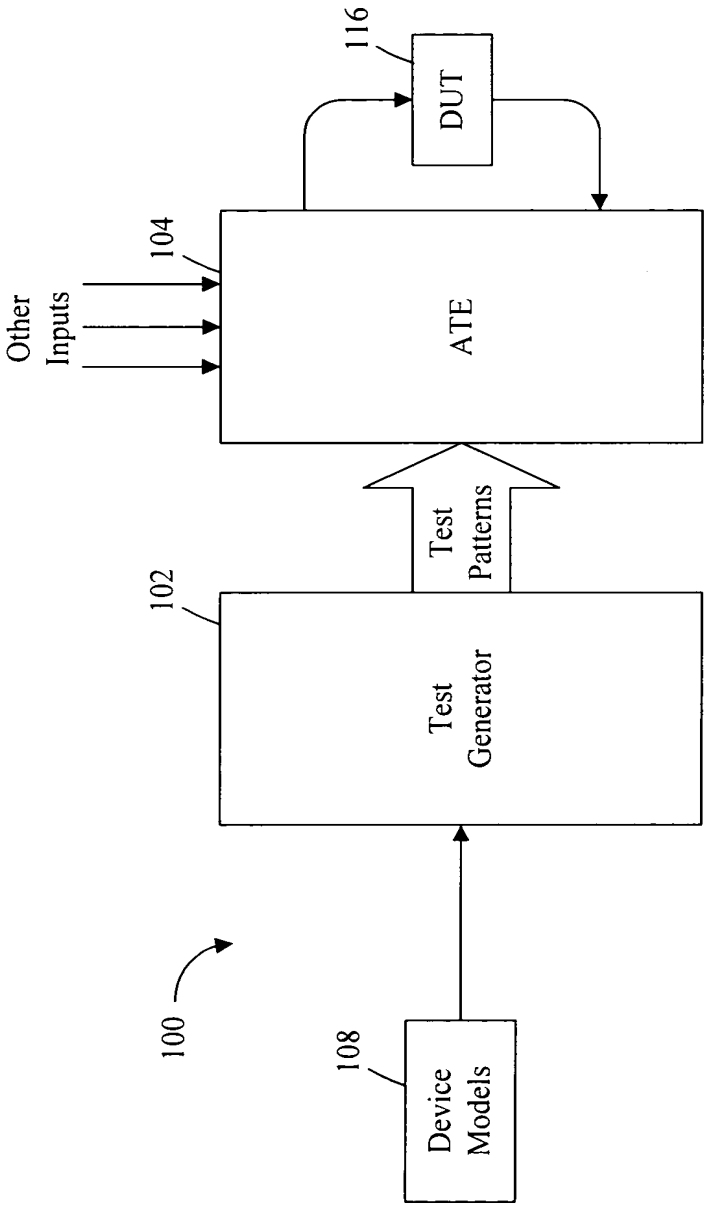

100
102
Test Generator
104
ATE
108
Device Models
116
DUT
Other Inputs
Test Patterns

FIG. 1

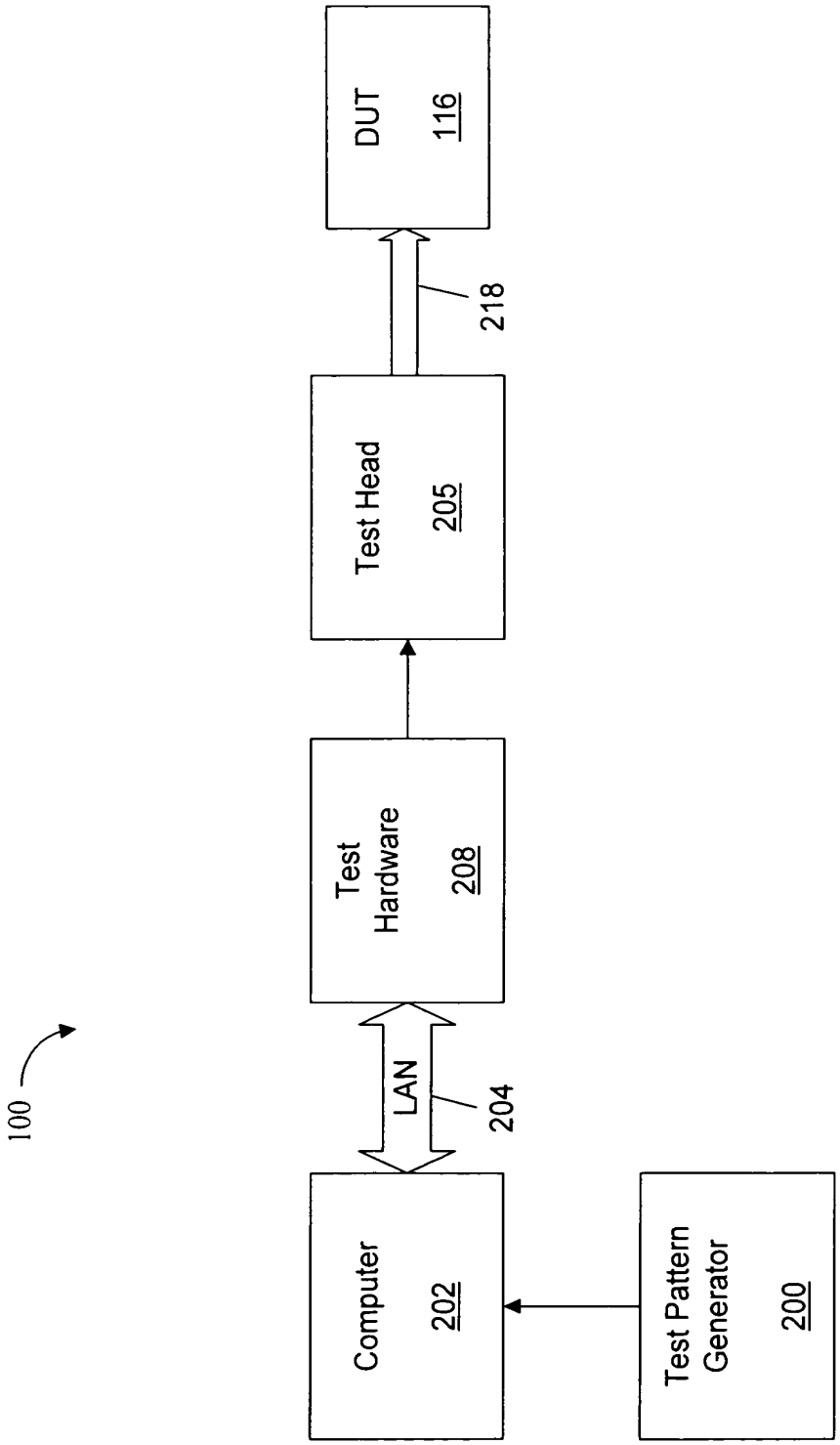

100
Computer
202
Test Pattern Generator
200
LAN
204
Test Hardware
208
Test Head
205
218
DUT
116

FIG. 2

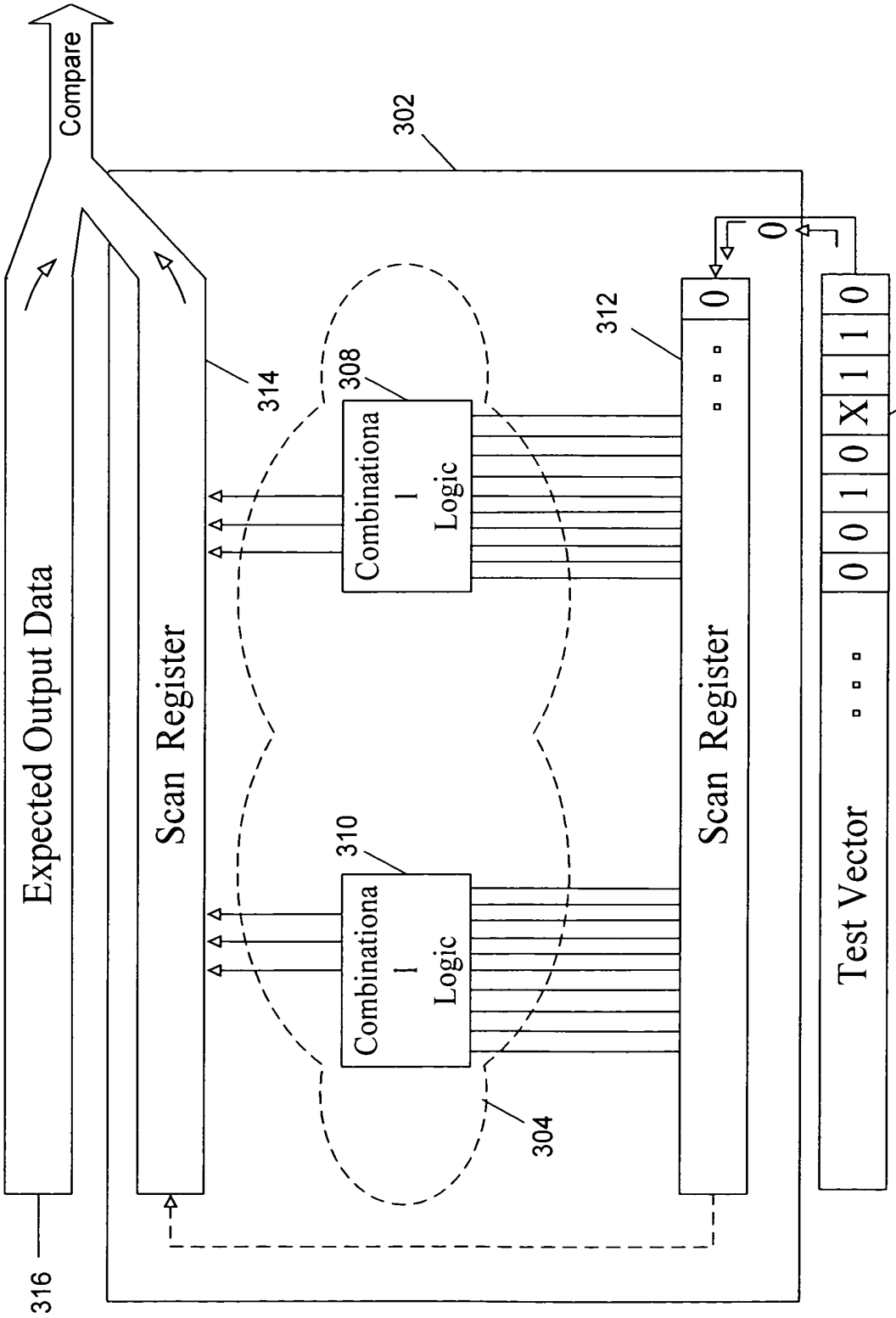

Compare
302
Expected Output Data
Scan Register
314
308
Combinationa
l
Logic
310
Combinationa
l
Logic
304
312
Scan Register
0
306
Test Vector
0 0 1 0 X 1 1 0
316

FIG. 3

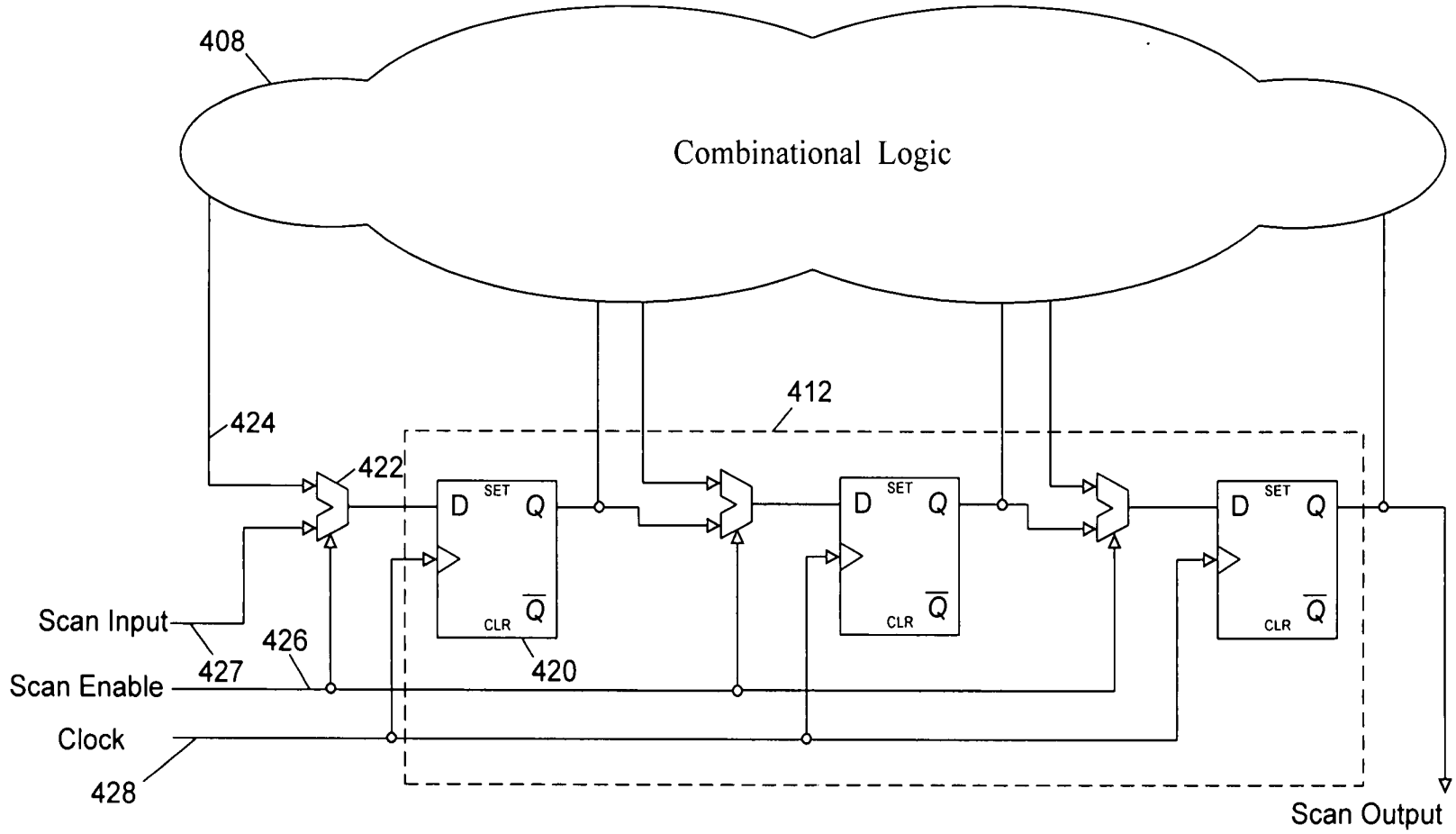

408
Combinational Logic
412
424
422
SET
D
Q
CLR
Q
Scan Input
427
426
Scan Enable
420
Clock
428
Scan Output

FIG. 4

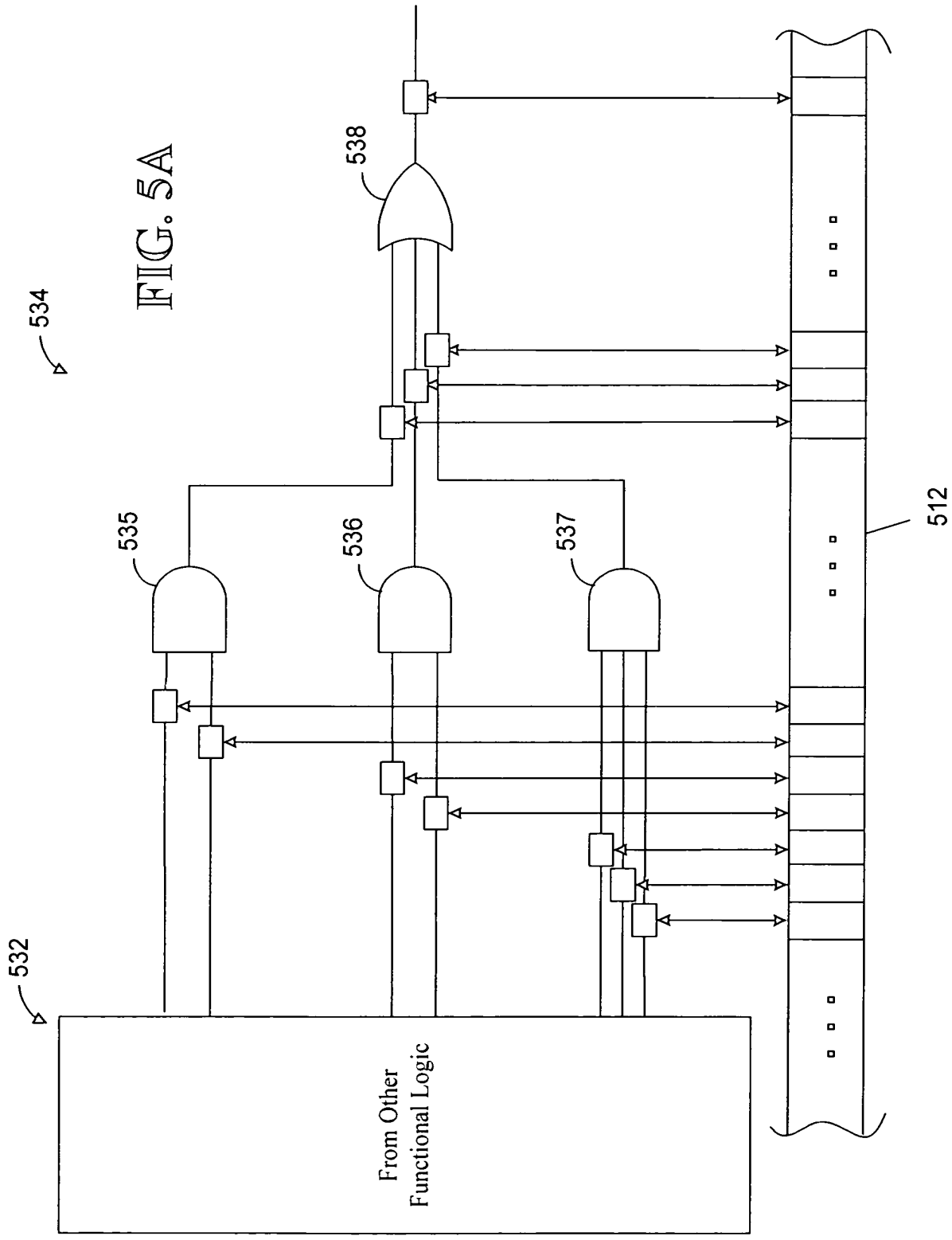


FIG. 5A

FIG. 5B

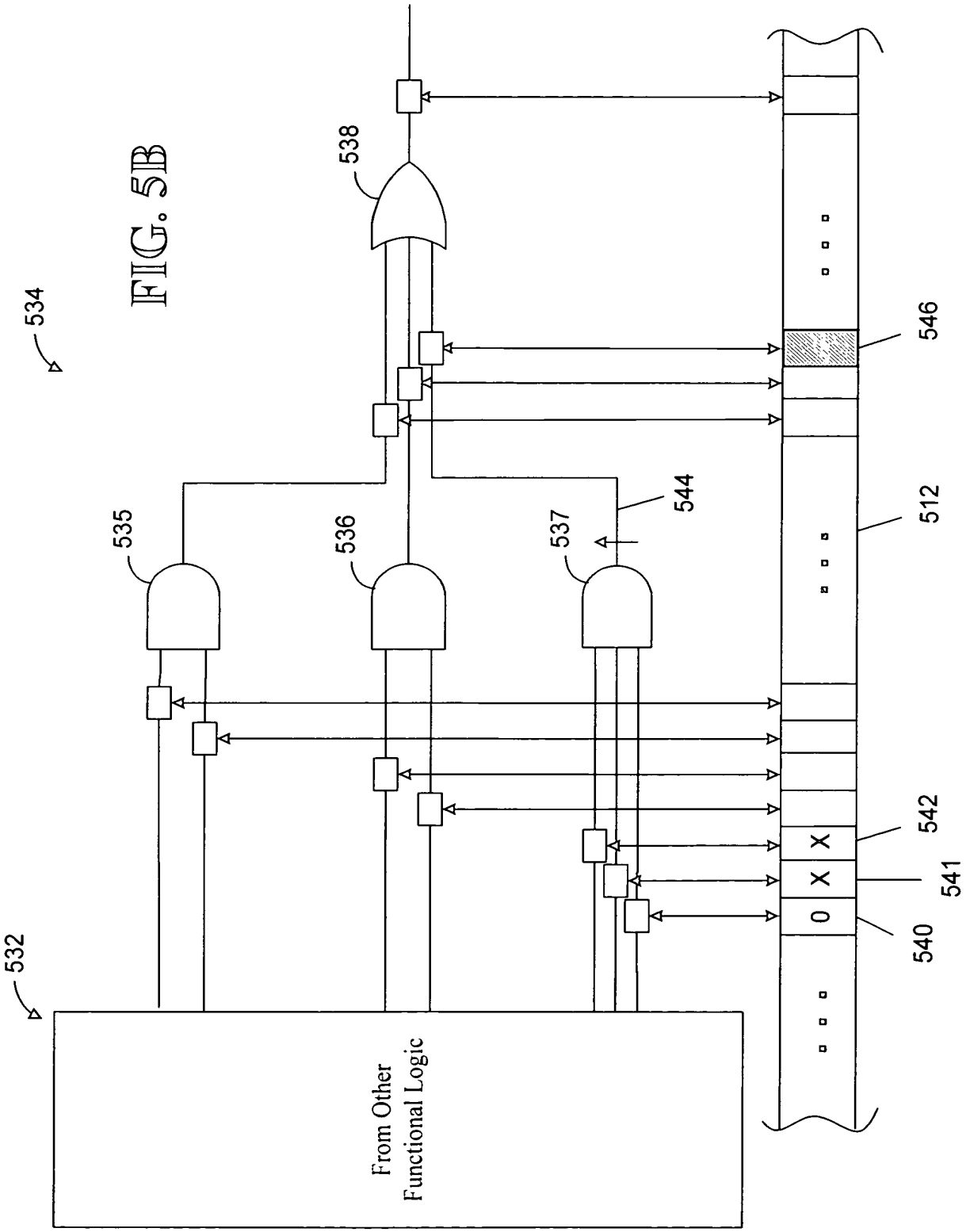
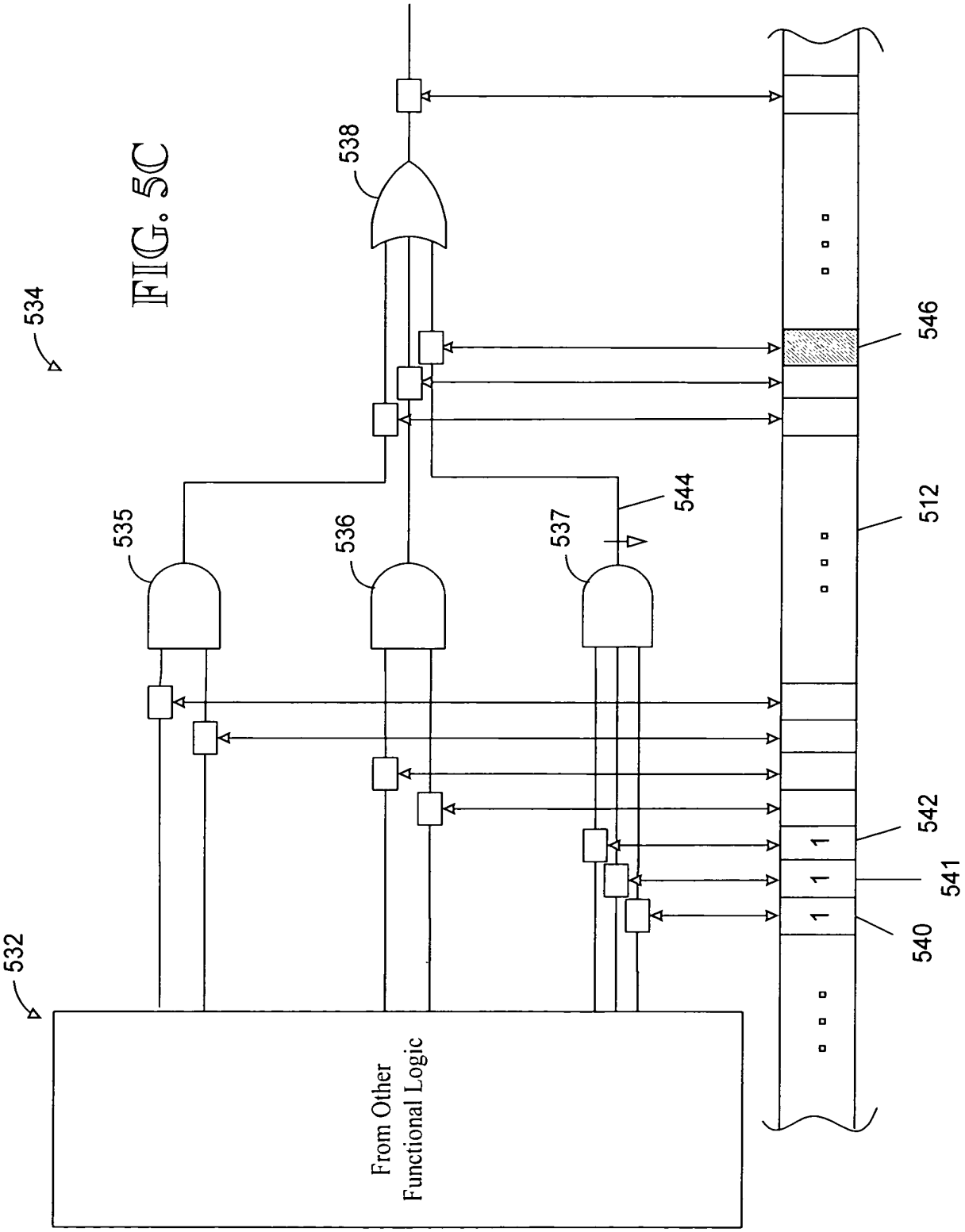

534
538
546
535
536
537
544
512
542
X
X
541
0
540
532
From Other
Functional Logic

FIG. 5C


532
534
535
536
537
538
540
541
542
544
546
512
From Other
Functional Logic
1
1
1

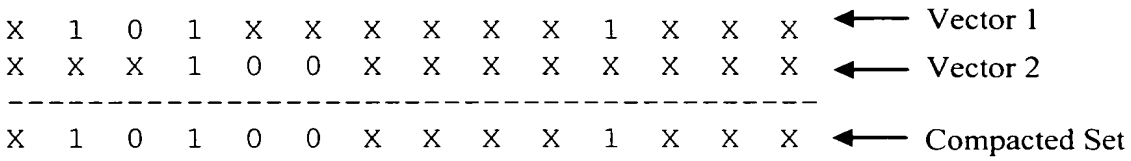


FIG. 6A

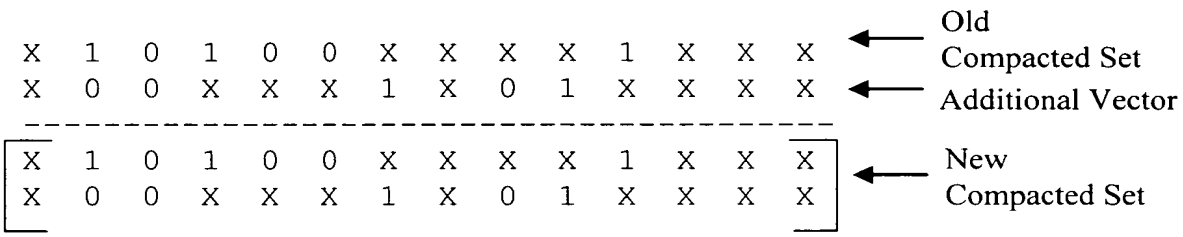


FIG. 6B

FIG. 6C

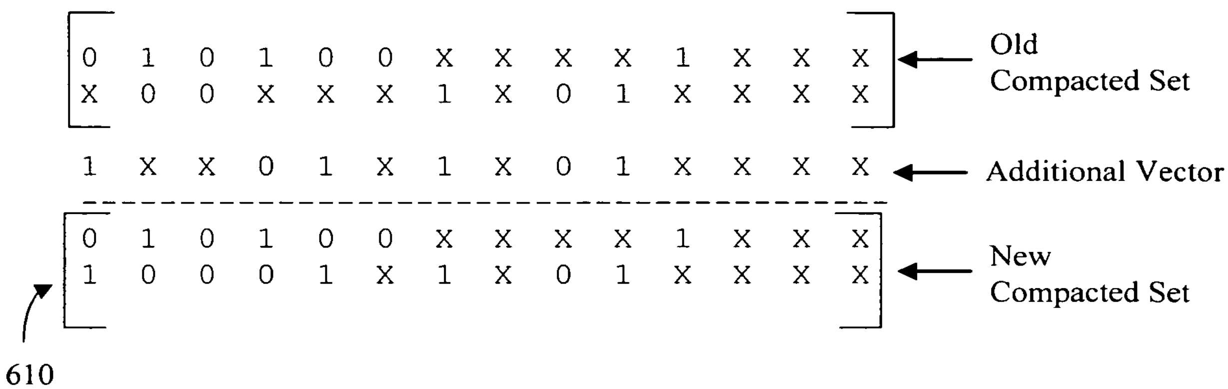


FIG. 6D

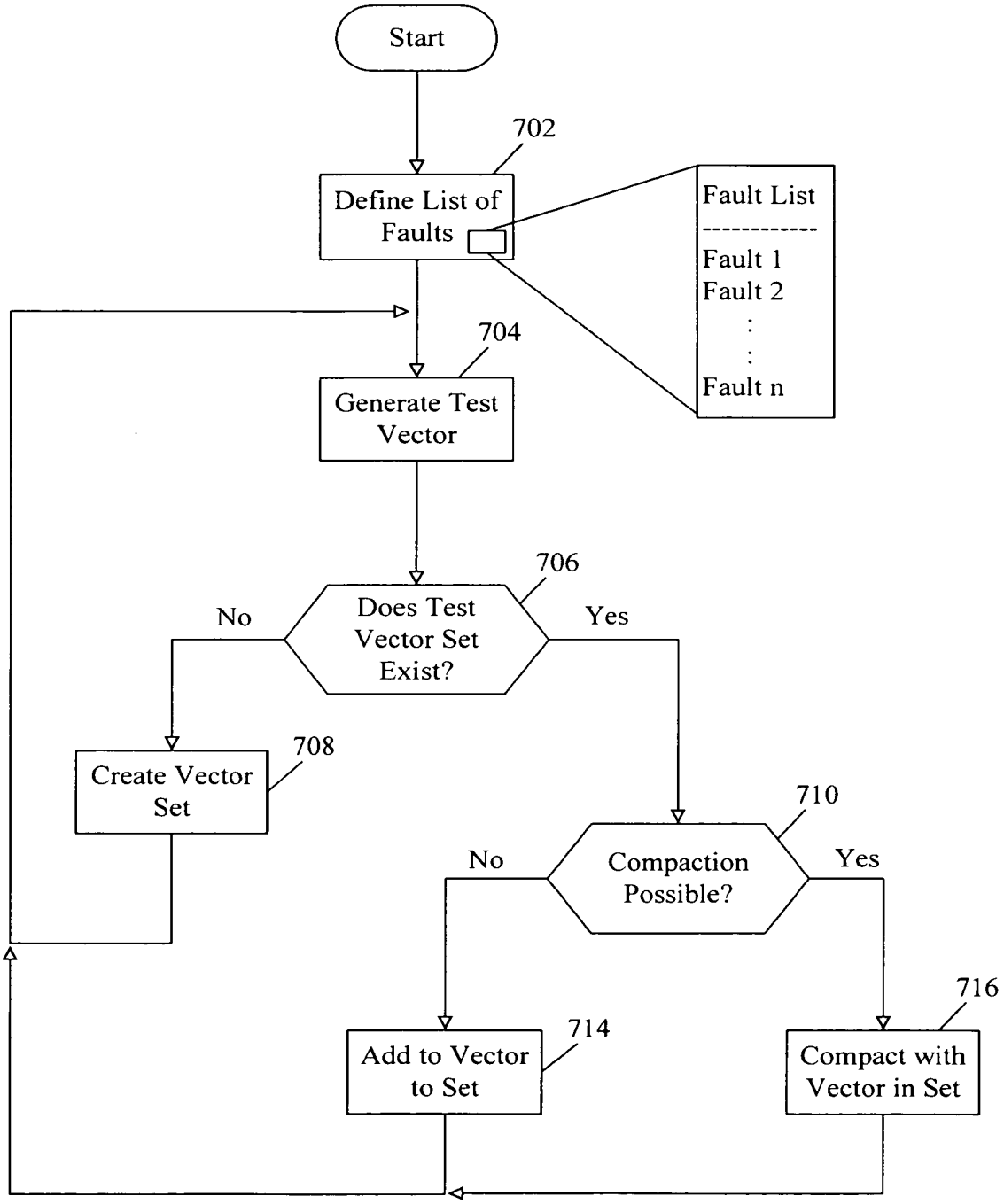

Start
702
Define List of Faults
Fault List
Fault 1
Fault 2
Fault n
704
Generate Test Vector
706
Does Test Vector Set Exist?
No
Yes
708
Create Vector Set
710
Compaction Possible?
No
Yes
714
Add to Vector to Set
716
Compact with Vector in Set

FIG. 7

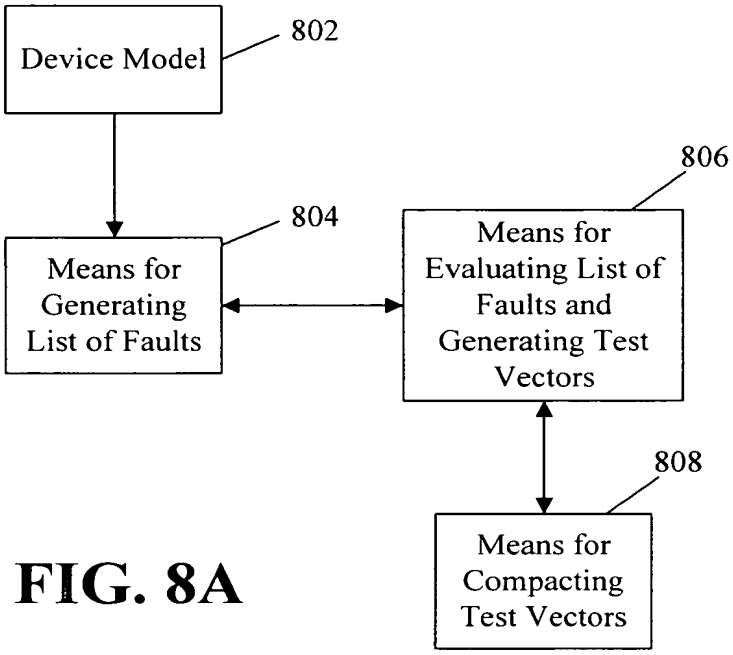

Device Model
802
806
804
Means for Generating List of Faults
Means for Evaluating List of Faults and Generating Test Vectors
808
Means for Compacting Test Vectors

FIG. 8A

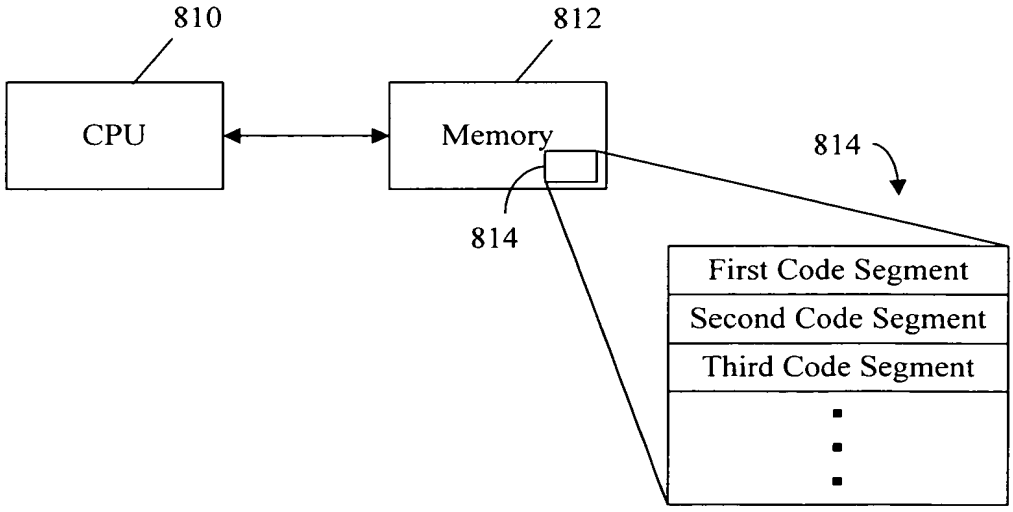

810
812
CPU
Memory
814
814
First Code Segment
Second Code Segment
Third Code Segment

FIG. 8B